REMARKS/ARGUMENTS

Claims 1-29 are pending in the present application.

This Amendment is in response to the Office Action mailed April 29, 2004. In the Office Action, the Examiner objected to the specifications and the drawings, rejected claims 1-29 under 35 U.S.C. §112; claims 1 and 11 under 35 U.S.C. §102(b); and claims 1-3, 4-7, 8-10, 11-13, 14-17, 18-20, 21-23 and 28-29 under 35 U.S.C. §103(a). Applicant has amended claim 21. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Specification

1. The Examiner objected to the abstract of the disclosure because the abstract is not descriptive enough, particularly the relationship between the circuit and the bus frequencies. Applicant respectfully disagrees.

The purpose of the abstract is to enable the United States Patent and Trademark Office and the public generally to determine quickly from a cursory inspection the nature and gist of the technical disclosure. 37. C.F.R. §1.72, MPEP 608.01(b). Excessive mechanical and design details of an apparatus should not be included in the abstract. MPEP 608.01(b).

The Abstract as written provides sufficient information for the United States Patent and Trademark Office and the public to determine quickly from a cursory inspection the nature and gist of the technical disclosure. The relationship between the circuit and the bus frequencies is provided in that the circuits are dynamically configured according to the bus frequency. No further details are necessary.

2. The Examiner objected to the specification due to minor informalities. In response, Applicant has amended the specification accordingly. Therefore, Applicant respectfully requests the objection be withdrawn.

Drawings

1. The Examiner objected to the drawings for not having the labels de-multiplexer in Figures 3A and 3B. In response, Applicant has amended Figures 3A and 3B. In addition, Applicant found additional typographical errors in Figure 2 and has amended accordingly. The

amended drawings are included in the Appendix. Therefore, Applicant respectfully requests the objection to the drawings be withdrawn.

Claim Objections

1. The Examiner objects to claim 21 because of minor informalities. In response, Applicant has amended claim 21 to add the missing word "to".

Accordingly, Applicant respectfully requests that the Examiner withdraw the objection to claim 21.

Rejection Under 35 U.S.C. § 112

1. In the Office Action, the Examiner rejected claims 1-29 under 35 U.S.C. §112, first paragraph, as being indefinite for failing to comply with the enablement requirement.

In stating the reason for the rejection, the Examiner states that claims 1, 11, and 21 do not enable one on how to dynamically configure the circuit according to the frequency of the coupled bus (Office Action, page 3, paragraph 6). Applicant respectfully disagrees.

There is no enablement requirement for a claim *per se*. The enablement requirement refers to the requirement of 35 U.S.C. §112, first paragraph that the specification describe how to make and how to use the invention. MPEP 2164. Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contain sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. MPEP 2164.01.

In order to make a rejection, the Examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. In re Wright, 999F.2d 1557, 1562, 27USPQ2d 1510, 1513 (Fed. Circ. 1993) (Examiner must provide a reasonable explanation as to why the scope of protection provided by a claim is not adequately enabled by the disclosure). Here, the Examiner has not pointed out any missing information in the disclosure that could have enabled the rejected claims.

Applicant contends that the specification provides ample support to enable one skilled in the art to make and use the claimed invention. Applicant respectfully directs the Examiner's attention to the Specification, paragraphs [0028] and [0029] where a discussion regarding dynamic configuration of the circuit is provided.

2. The Examiner rejected claims 1-29 under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential elements. The Examiner further states that the control circuit is the omitted element. Applicant respectfully disagrees.

First, a claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record may be rejected under 35 U.S.C. §112, first paragraph, as not enabling. MPEP 2172.01. Omission of essential elements is therefore governed by 35 U.S.C. §112, first paragraph, not second paragraph.

Second, to fall within the pur view of 35 U.S.C. §112, first paragraph, the omitted matter must be disclosed to be essential to the invention as described in the specification or in other statements of record, not merely by a subjective opinion of the Examiner.

Third, even if a claim which omits matter disclosed to be essential, the Examiner still has to prove that this omission amounts to not enabling.

Here, the control circuit is not disclosed to be essential to the invention as described in the specification or in other statements of record.

Therefore, Applicant respectfully requests the rejection under 35 U.S.C. §112 be withdrawn.

Rejection Under 35 U.S.C. § 102

1. In the Office Action, the Examiner rejected claims 1 and 11 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,047,349 issued to Klein ("Klein"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of anticipation. As the Examiner may be aware, to anticipate a claim, the reference must teach every element of a the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989).

Klein discloses a system for communicating through a computer system bus bridge. A system controller includes a CPU bus data path, a PCI bus data path, and other circuits (Klein,

col. 5, lines 5-21). An ISA bridge immediately responds to a corresponding address placed on the PCI bus by the system controller (Klein, col. 5, lines 52-56). The system controller and the ISA bridge communicate and exchange data according to PCI protocols (Klein, col. 6, lines 5-7).

Klein does not disclose, either expressly or inherently, (1) a delayed transaction (DT) data, (2) an input circuit being dynamically configured according to a bus frequency, (3) an output circuit to transfer the DT data to a second bus, and (4) the output circuit being dynamically configured according to the bus frequency.

First, the Examiner states that the structure of 108 in Figure 4 of Klein discloses the buffers. However, the structure 108 is merely a memory to store data, not DT data. Second, the PCI bus data path (element 122 in Figure 5) is not equivalent to an input circuit. It is part of a data path controller (Klein, col. 5, lines 12-16). It is not dynamically configured according to the bus frequency. Third, the CPU bus data path (element 120 in Figure 5) is not equivalent to an output circuit. It is also part of a data path controller (Klein, col. 5, lines 12-16), and it is not dynamically configured according to the bus frequency. Since the PCI bus data path is interfaced to the PCI bus and the CPU bus data path is interfaced to the CPU bus, they do not correspond to one bus frequency.

Therefore, Applicant believes that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejection under 35 U.S.C. §102(b) be withdrawn.

Rejection Under 35 U.S.C. § 103

1. In the Office Action, the Examiner rejected claims: (1) 1-3, 8-10, 11-13, and 18-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,941,970 issued to Lange ("Lange") in view of U.S. Patent No. 5,857,082 issued to Murdoch et al. ("Murdoch"), (2) 4-7 and 14-17 under 35 U.S.C. §103(a) as being unpatentable over Lange in view of Murdoch, and further in view of U.S. Patent No. 4,684,829 issued to Uratani ("Uratani"), and (3) 21-23 and 28-29 under 35 U.S.C. §103(a) as being unpatentable over Klein, in view of Lange, and further in view of Murdoch. Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness. As the Examiner is aware, to establish a *prima facie* case of obviousness, three basic criteria must be

met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., rev. 2, May 2004).* Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Lange discloses an address/data queueing arrangement and method for providing high data through-put across bus bridge. A bus interface bridge circuit transfers commands from an initiating bus to a target bus (Lange, col. 3, lines 4-6). An initiating bus interface outputs a plurality of commands. A memory array is coupled to the initiating bus interface to receive the commands. The memory array may be a FIFO queue. A plurality of retry registers, each coupled to the initiating bus to receive a different one of the commands. Each retry register is also coupled to the FIFO queue to re-enter the commands that are not completed successfully (Lange, col. 3, lines 19-21).

Murdoch discloses a method and apparatus for quickly transferring data from a first bus to a second bus. A bridge couples a first bus to a second bus. The bridge includes a buffer to store two data elements of a first packet transferred to the buffer for the first bus and a controller to allow a first data element to be transferred from the buffer to a second bus (Murdoch, col. 5, lines 6-9, 26-29).

Uratani discloses a CMOS tree decoder with speed enhancement by adjustment of gate width. A semi-conductor decoder circuit includes PMOS transistors to sections and NMOS transistor section in which NMOS transistors are connected at subsequent stages of the 2^{N-1} number of PMOS transistor sections in the form of a tree structure (Uratani, col. 3, lines 40-54).

Klein discloses a system for communicating through a computer system bus bridge as discussed above.

Lange, Murdoch, Uratani and Klein, taken alone or in any combination, does not disclose, suggest, or render obvious (1) a delayed transaction (DT) data, (2) an input circuit being dynamically configured according to a bus frequency, (3) an output circuit to transfer the DT data to a second bus, and (4) the output circuit being dynamically configured according to the

bus frequency. There is no motivation to combine Lange, Murdoch, Uratani and Klein because none of them addresses the problem of dynamic delayed transaction buffer configuration based on bus frequency. There is no teaching or suggestion that a delayed transaction is present. Lange, read as a whole, does not suggest the desirability of dynamically configuring an input circuit and an output circuit.

Lange merely discloses transferring commands, not DT data. The initiating bus interface and the target bus interface are not dynamically configured according to a frequency. Murdoch merely discloses transferring a data element from a first bus to a buffer and from the buffer to a second bus. There is no dynamic configuration according to the bus frequency. Combining Lange and Murdoch at best merely leads to transferring commands from one bus to another bus. Uratani merely discloses a tree structure in a semiconductor decoder circuit, not a bus system. Uratani does not discloses demultiplexer and multiplexer circuits used for dynamic configuration according to bus frequency. Furthermore, Uratani is a non-analogous art. Persons skilled in the art of bus interface circuit do not consult semiconductor decoder technology. Klein, as discussed under the 35 U.S.C. 102(b) above, does not disclose or suggest any elements as recited in claims 1, 11, and 21.

In the present invention, the cited references do not expressly or implicitly suggest (1) a delayed transaction (DT) data, (2) an input circuit being dynamically configured according to a bus frequency, (3) an output circuit to transfer the DT data to a second bus, and (4) the output circuit being dynamically configured according to the bus frequency. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Lange, Murdoch, Uratani and Klein is an obvious application of dynamic delayed transaction buffer configuration based on bus frequency.

Therefore, Applicant believes that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. §112, 35 U.S.C. §102(a), and 35 U.S.C. §103(b) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: June 28, 2004 By _____

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